A Fully Integrated 5.8 GHz U-NII Band 0.18-μm CMOS VCO

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***Abstract*—A fully integrated 5.8 GHz CMOS L-C tank voltage-controlled oscillator (VCO) using 0.18-μm 1P6M standard CMOS process for 5 GHz U-NII band WLAN application is presented. The VCO core circuit uses only PMOS to pursue a better phase noise performance since it has less $1/f$ noise than NMOS. The measurement is performed by using a FR-4 PCB test fixture. The output frequency of the VCO is from 5860 to 6026 MHz with a 166 MHz tuning range and the phase noise is −96.9 dBc/Hz at 300 KHz (or −110 dBc/Hz at 1 MHz) with $Vctrl = 0$ V. The power consumption of the VCO excluding buffer amplifiers is 8.1 mW at $V_{DD} = 1.8$ V and the output power is −4 dBm.**

***Index Terms*—0.18 μm, 5.8 GHz, 802.11a, CMOS, VCO, WLAN.**

I. Introduction

DUE TO the rapidly growing demand for broad band wireless communication, communication band is moving toward 5 GHz U-NII band, such as IEEE 802.11a wireless LAN (WLAN) which can provide a maximum data rates of 54-Mbit/s. Requirement of low power and low cost pushes the trend toward single radio chip. Fully integrated voltage-controlled oscillator (VCO) is one of the most important and challenging building blocks in a RF transceiver. With the demand for low power and low cost, on-chip VCO with no external component is the best choice. However, the low Q on-chip passive component such as inductor will degrade the VCO phase noise performance.

Recently, researches on 5 GHz VCO have been reported [1]–[6]. In [1], a 5 GHz CMOS VCO covering from 4.2 to 5.05 GHz with 18% tuning range has been reported. This VCO is designed to be frequency-divided to two I and Q LO signals for 2.4 GHz direct conversion or low-IF receivers. Hence, wider tuning range is necessary after frequency division. In [2], a 5.8 GHz fully integrated 0.25-μm CMOS LC VCO has been reported. This VCO achieved −112 dBc/Hz at 100 MHz offset with a tuning range of 810 MHz. In our research, for 802.11a WLAN application (5.725∼5.825 GHz), with the selected IF 200 MHz and the high side injection LO, the VCO output frequency should cover 5925∼6025 MHz with about 1.7% tuning range. Hence in this 5 GHz VCO, we have designed to have about 2 to 3% tuning range which will be enough for application. Also, it is because wider tuning range implies higher tuning sensitivity and hence more sensitive to the noise comes from control path.

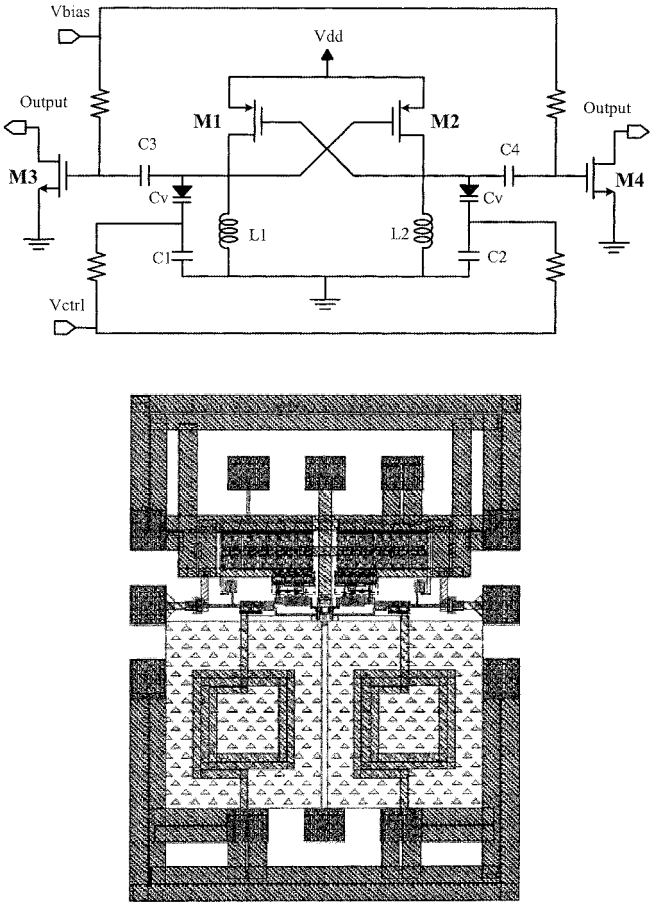

Fig. 1. Circuit schematic and layout of a 5.8 GHz L–C tank CMOS VCO.

This paper presents a fully integrated 5.8 GHz VCO fabricated in a TSMC 0.18-μm standard CMOS process. Low dc voltage and power consumption, simple circuit scheme, and satisfactory phase-noise performance are design goals.

II. Circuit Design

The flicker noise ($1/f$) of a transistor is the cause of the close-in phase noise near the carrier in $1/f^3$ shape. In the CMOS process, the transistor $1/f$ noise is generally high and causes serious degradation of VCO phase noise performance. However, the PMOS $1/f$ noise is usually smaller than NMOS in one order of magnitude. An active port with low $1/f$ noise will reduce not only the magnitude of phase noise in $1/f^3$ and $1/f^2$ region, but

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also lower down the corner frequency between $1/f^3$ and $1/f^2$ region. To attain a better phase noise performance PMOS transistors were used in the VCO core [6]. A VCO circuit shown in Fig. 1 (top) has a cross-coupled connection of PMOS transistors M_1 and M_2 to form a positive feedback loop for providing negative resistance to compensate the loss in the L–C tank. The source and gate voltage of M_1 and M_2 is directly biased at 0 V and V_{DD} (1.8 V), respectively, without any extra current source. This bias scheme reduces the transistor's width requirement for oscillation starting and maximizes the oscillator signal peak-to-peak amplitude. The supply voltage of 0.18-μm standard CMOS process is 1.8 V that is fairly low. If the cross-coupled pair is biased via current source, the allowable oscillator voltage swing will be further restricted and cause a poorer phase noise performance. According to Leeson–Cutler phase noise model [7] the phase noise which is single-sideband-noise to carrier ratio is inversely proportional to the signal power. For low supply voltage (1.8 V) operation, to enlarge the voltage swing by removing the use of current source, which reduces the voltage headroom, is one of the most direct ways to improve the phase noise performance. It is known that the VCO oscillation condition could be easily influenced by V_{DD}, which is the drawback of this bias scheme. However, for low supply voltage (1.8 V) in 0.18-μm CMOS process, it is a way to achieve a satisfied phase noise performance.

For further suppression of the phase noise in $1/f^3$ region caused by MOS $1/f$ noise, it needs to make the oscillation waveform as odd-symmetric as possible. Refer to [7], [8], the $1/f$ noise of active device will be upconverted to become $1/f^3$ noise when the VCO waveform is not sufficiently odd-symmetric. Therefore, the waveform symmetry needs to be carefully considered in VCO design, especially in such a high $1/f$-noise device as MOS.

As shown in Fig. 1, an L–C resonator is formed by on-chip spiral inductors (L_1 and L_2), p$^+$/n-well junction varactors (C_v) and capacitors (C_1 and C_2). The Q-factor of the tank circuit is primary limited by the inductor of which the Q value is about 10 between 5 to 6 GHz. Inductors of about 2.3 nH are formed by using 2.5 turns rectangular spirals with thick AlCu metal (metal-6 in 0.18-μm process). Series connected C_1–C_v and C_2–C_v, resonating with L_1 and L_2 respectively, determines the oscillation frequency. The VCO output frequency was tuned by applying control voltage 0$\sim$1.8 V at n-well port of the reverse biased junction varactors. M_3 and M_4 transistors form open drain buffer amplifiers in order to drive the 50 Ω test system such as spectrum analyzer. The layout of the VCO is shown in Fig. 1 (bottom). It is fabricated in 0.18-μm CMOS process with a chip area of 790 $\times$ 1020 μm^2 including pads.

III. Measured Results

Aglient ADS is used for design simulation of the VCO. The measurement is performed on a FR-4 PCB test fixture. VCO chip is connected to the test board by aluminum bond-wires. Effects of bond-wires and the FR-4 test board were all taken into account in simulation. While lower down the output signal level, bond-wires and the FR-4 test board do not effect the oscillation frequency and phase noise performance. VCO core and each buffer amplifier dissipate 8.1 mW and 22.5 mW, respectively, at a 1.8 V V_{DD}. As shown in Fig. 2, the measured oscillation frequency of the VCO covers from 5860 to 6026 MHz when control voltage is 0 to 1.8 V together with simulation results. The measured output power is about -4 dBm, as shown in Fig. 3 with a simulated value of about -2 dBm. The measured phase noise, as shown in Fig. 4, is -96.9 dBc/Hz

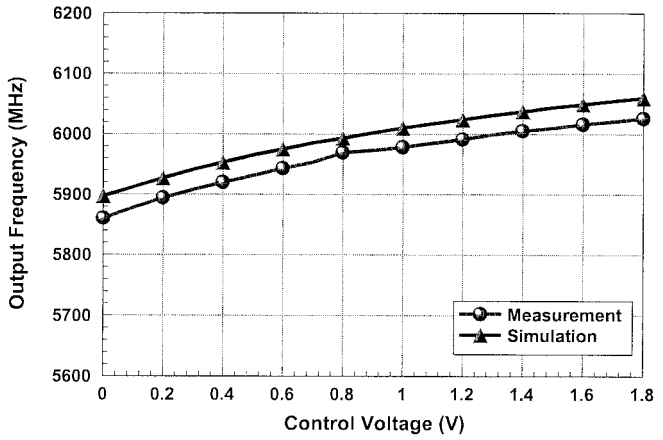

Fig. 2. Simulation and measurement of the 5.8 GHz VCO output frequency versus control voltage.

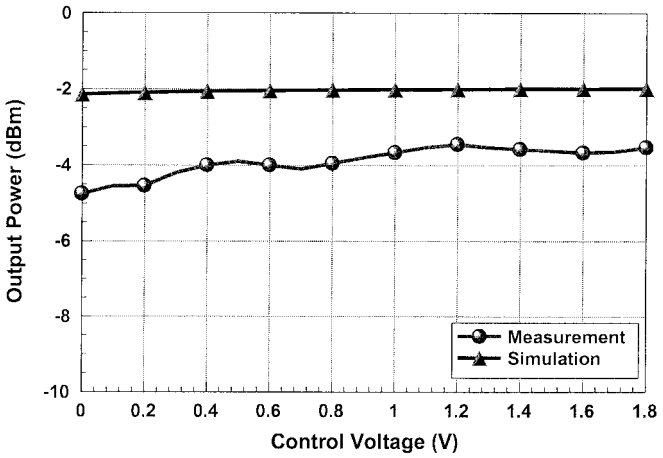

Fig. 3. Simulation and measurement of the 5.8 GHz VCO output power versus control voltage.

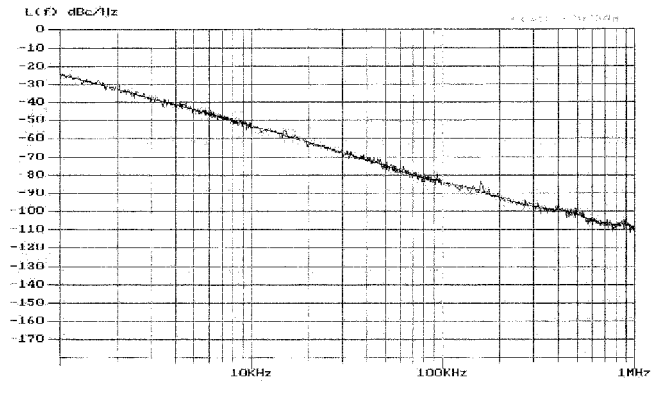

Fig. 4. Measurement of the 5.8 GHz VCO phase noise $Vctrl = 0$ V (-96.9 dBc/Hz at 300 KHz; -110 dBc/Hz at 1 MHz).

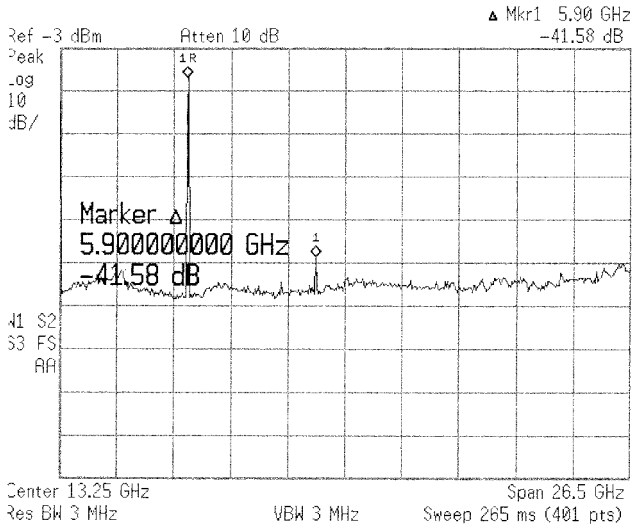

Fig. 5. Measurement of the 5.8 GHz VCO output spectrum. Power difference between fundamental and second harmonic is −41.6 dBc.

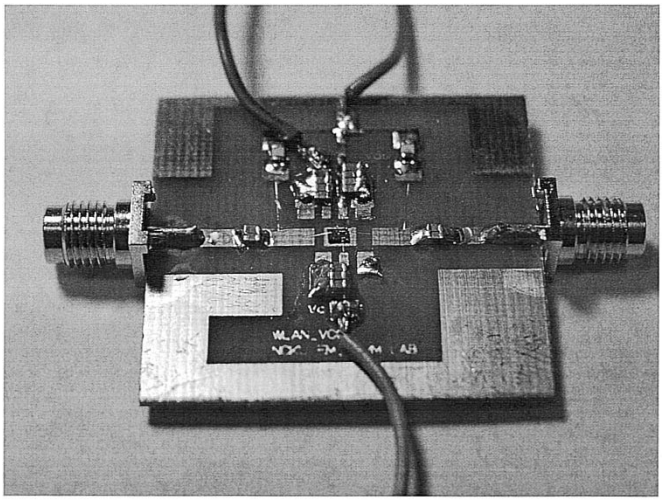

Fig. 6. Photograph of the 5.8 GHz CMOS VCO on a FR-4 PCB test fixture.

at 300 KHz (or −110 dBc/Hz at 1 MHz) with $Vctrl = 0$ V and −98.6 dBc/Hz at 300 KHz (or −111.5 dBc/Hz at 1 MHz) with $Vctrl = 1.8$ V, respectively. It seems a quite flat response of phase noise performance versus control voltage can be expected. Note that when VCO phase noise measurement is performed with the control voltage at 0 V, VCO has the highest K_{VCO}(∼180 MHz/V) among the tuning range. The above free running measurement of the phase noise performance shows that the fully integrated VCO is sufficient for wireless communication uses. When the VCO is utilized in 5 GHz frequency synthesizer application, the phase noise can be further suppressed by the loop filter of PLL frequency synthesizer. Fig. 5 shows the measured output spectrum of the VCO. The second harmonic is lower than fundamental tone by 41.6 dBc. The photo of the FR-4 PCB test fixture is shown in Fig. 6. Table I summarizes the measured performance of the designed 5.8 GHz CMOS VCO.

TABLE I
MEASURED PERFORMANCE OF A 5.8 GHz 0.18-μm CMOS VCO

5.8 GHz 0.18-μm CMOS VCO	
Control Voltage	0V ~ 1.8V
Bias Current	4.5mA
Buffer Amp Bias Current (Each)	12.5mA
Turning-range	5860~ 6026 MHz
Tuning Sensitivity	50 ~ 180 MHz /V
Phase Noise (with Buffer Amp)	Vctrl=0V : -96.9dBc/Hz@300kHz, -110dBc/Hz@1MHz Vctrl=1.8V: -98.6dBc/Hz@300KHz, -111.5dBc/Hz@1MHz
Pushing Figure	−1MHz@0.2V, 3.3MHz@-0.2V
Output Power	-4dBm
Die size	790 x 1020μm^2

IV. CONCLUSION

A fully integrated 5.8 GHz L–C tank VCO fabricated in a TSMC 0.18-μm standard CMOS process is presented. Low dc voltage and power consumption, simple circuit scheme, and satisfactory phase-noise performance are design goals. For IEEE 802.11a WLAN application (5.725∼5.825 GHz), with the selected IF 200 MHz and the high side injection LO, the VCO output frequency covers from 5925 to 6025 MHz with 1.7% tuning range. The VCO core circuit using only PMOS to achieve better phase noise performance. VCO output frequency is tuned by on-chip p^+/n-well junction varactors. Measurement is performed by using a FR-4 PCB test fixture. The output frequency of the VCO is from 5860 to 6026 MHz with a 166 MHz tuning range (about 2.8%) and the output power is −4 dBm. The phase noise is −96.9 dBc/Hz at 300 KHz (or −110 dBc/Hz at 1 MHz) with $Vctrl = 0$ V and −98.6 dBc/Hz at 300 KHz (or −111.5 dBc/Hz at 1 MHz) with $Vctrl = 1.8$ V, respectively. The pushing figure is −1 MHz at 0.2 V and 3.3 MHz at −0.2 V. The VCO excluding buffer amplifiers consumes 8.1 mW at a 1.8 V V_{DD}. Low power consumption of the VCO suggests that 0.18-μm CMOS process is well capable for 5.8 GHz WLAN application.

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